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TO: EXAMINER: JOHN J. TABONE, JR. (ART UNIT 2133)

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FROM: PAUL J. DITMYER, ESQ.

DATE: September 19, 2005

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COMMENTS/INSTRUCTIONS:

Please see attached Appeal Brief for Application Serial No. 10/075,113.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of:
REAUJOIN ET AL.

Serial No. **10/075,113**
JR

Confirmation No: **6957**

Filing Date: **FEBRUARY 13, 2002**

For: **METHOD OF TESTING A SEQUENTIAL ACCESS MEMORY PLANE AND A CORRESPONDING SEQUENTIAL ACCESS MEMORY SEMICONDUCTOR DEVICE**

Examiner: **J. TABONE,**

Art Unit: **2133**

APPELLANT'S APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief together with the requisite fee of $500.00 for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484**.

(1) Real Party in Interest

The real party in interest is STMicroelectronics SA.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

(3) Status of the Claims

Claims 9-31 are pending in the application, all of which being appealed herein.

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(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

In general, the invention is directed to testing a sequential access memory array with a particularly simple implementation leading to an extremely small overall size of the test logic.

Referring to FIG. 1 (reproduced below) and page 5, line 12 through page 8, line 19 of the specification, for example, the presently claimed invention will now be described.

The invention of indpendent Claims 9 and 11 provides a method of testing a sequential access memory plane PMM adapted to store words each made up of bits. In the method, test words each made up of test bits DT are written in the memory array. The test words are sequentially extracted from the memory plane and the test bits of the extracted words are compared with expected binary data bits DAi, so that for each test word extracted, the corresponding test bits are compared sequentially with n respective expected data bits before extracting the next test word.

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FIG.1

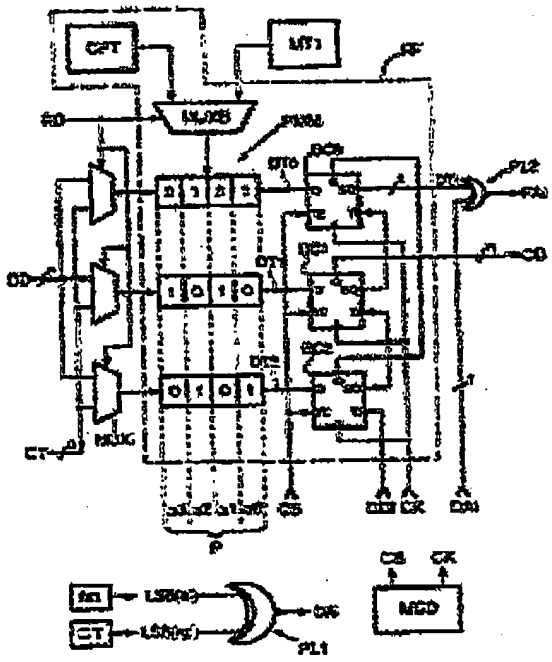

FIG. 1 of the Present Application.

Figure 1 shows a sequential access memory device FF, for example an FIFO memory. The memory FF includes a memory array PMM able to store p words each of n bits. In other words, the depth of the memory is equal to p and the width of the data bus is equal to n. In the example described here, for simplicity, p = 4 and n = 3. The figure shows the successive storage addresses ai of the p words in the memory array PMM.

In the normal operating mode writing and reading are effected in the conventional manner using write and read pointers controlled in the conventional manner by control circuit/means CPT. A multiplexer MUXB controls the write and read pointers of the memory array in response to a control

signal RB from either the control means CPT (in the normal mode of operation) or the test mode control circuit/means MT1 (in the test mode of operation). Similarly, the data to be written into the memory array is selected via n multiplexers MUXi which are also controlled by the control signal RB.

Accordingly, in the normal mode of operation, the n data bits DD on the bus are written into the memory array. In the test mode of operation, on the other hand, binary test data bits DT are written into the memory plane PMM.

The control means or control circuit MT1 and the multiplexers MUXi and MUXB then form first test circuit or means used, in conjunction with the test data bits DT, to write into the memory array p test words each made up of n test bits. Also, in a preferred embodiment, the first test means write the p test words of n bits in such a way as to obtain a checkerboard test configuration in the memory plane. A checkerboard configuration, as shown in Figure 1, is one in which each test word includes alternating 0 and 1 bits, and wherein the 0 bits and the 1 bits of two words written at successive addresses are mutually shifted by one bit.

The memory FF further includes n output registers BC0-BC2. Here the output registers are D-type flip-flops each having a data input D connected to one of the n outputs of the memory plane PMM. Each flip-flop D also has a test input TI, a test output SO and a test control input TE. Furthermore, each flip-flop is clocked by a clock signal CK. Finally, each flip-flop has a data output Q.

In the normal mode of operation the n data bits extracted from the memory PMM are delivered to the respective n data inputs D of the flip-flops and then to the n data outputs Q in time with the rising edges of the clock signal CK. This is not the case in the test mode of operation, however, as explained next in more detail.

As well as being connected to n respective outputs of the memory plane PMM by their data input D, the n flip-flops are chained. To be more precise, the test output SO of one flip-flop, for example the flip-flop BC1, is connected to the test input TI of the adjacent flip-flop, here the flip-flop BC0, for example, to form a chain. The test input TI of the first flip-flop BC2 in the chain recieves an initial data bit DDI.

All the test control inputs TE receive a signal CB from the control means or control circuit MCD. When the signal CB takes the value 0, for example, it constitutes a first control signal and a data bit at the input D of a flip-flop is then delivered to the output SO on the next rising edge of the clock CK. On the other hand, when the signal CB takes the value 1, it constitutes a second control signal and, in this case, each flip-flop delivers the data bit at the test input TI to the output SO in time with the rising edges of the clock signal CK.

A comparator or comparator means are further provided, here in the form of a EXCLUSIVE NOR logic gate PL2. A first input of the logic gate PL2 is connected to the test output SO of the flip-flip BC0 at the end of the chain. The other input of the logic gate PL2 receives the expected data bits DAi sequentially. The output of the logic gate PL2 is a logic signal that takes the value 0 or 1 in time with the comparison operations and as a function of their result.

A counter CT, incremented in time with the clock signal CK, counts from 0 to n - 1. Assuming that the value 0 is representative of the rank of the test bit DT0, the least significant bit of the value of the counter is equal to 0 for the test bit DT0, 1 for the test bit DT1, and 0 for the test bit DT2. Logically combining the least significant bit LSB (ai) of the read address and the least significant bit LSB

(rgi) of the counter value in the EXCLUSIVE NOR logic gate PL1 supplies sequentially the values 1, 0 and 1 corresponding to the test word at the address a0 in the memory plane PMM. If the test word stored at the address a0 had been 0 1 0, the logic gate PL1 would simply have been an EXCLUSIVE OR gate.

Independent Claims 14 and 20 are directed to a sequential access semiconductor memory device including a memory array PMM for storing words each made up of bits, and test logic connected to the memory array. The test logic includes a first test circuit or means MT1, MUXi, MUXB for writing test words each having test bits in the array, and a second test circuit or means Bci, MCD, PL2 (page 6, line 12 through page 7, line 27 of the specification) for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

Similarly, independent Claim 26 is directed to a test circuit for a sequential access semiconductor memory device having a memory array PMM. The test circuit includes a first test circuit MT1, MUXi, MUXB for writing test words each having a plurality of test bits in the array, and a second test circuit Bci, MCD, PL2 for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

(6) Grounds of Rejection to be Reviewed On Appeal

Claims 9, 11, 14-17, 20-23 and 26-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Kim et al. (U.S. Patent No. 6,108,802) in view of Martens (U.S. Patent No. 5,751,727); Claims 10, 12, 13, 18, 24, 29 and 30 stand rejected under 35 U.S.C. § 103(a) as being

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unpatentable over the combination of Kim et al. in view of Martens and further in view of Zorian et al. (U.S. 6,330,696); Claims 19, 25 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Kim et al. in view of Martens and Zorian et al. and further in view of Biskup et al. (U.S. 6,751,757).

Claims 9-17, 20-23 and 26-29 stand together as a group. Claims 18, 24 and 30 stand together as a group and separately from Claims 9-17, 20-23 and 26-29 for the reasons provided below. Claims 19, 25 and 31 stand together as a group and separately from the other groups for the reasons provided below.

(7) Argument

Claims 9-31 were rejected in view of Kim et al. (US Patent No. 6,108,802) in view of Martens (US Patent No. 5,751,727) taken together or in combination with Zorian et al. (U.S. 6,330,696) and/or Biskup et al. (U.S. 6,751,757) for the reasons set forth on pages 2-11 of the final Office Action. Appellants contend that Claims 9-31 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §103 is requested.

Indpendent Claims 9, 11, 14, 20 and 26 are Patentable Over Kim et al. in view of Martens

The independent claims include testing a sequential access memory plane by writing p test words each made up of n test bits in the memory array, and then extracting the p test words sequentially from the memory plane to compare with expected binary data bits. It is this combination of features which is not fairly taught or suggested in the cited references and which patentably defines over the cited

references.

In the Kim et al. patent, a variety of FIFOs, including single and dual port, RAM-type and/or having a ring type addressing mechanism, are tested by causing the FIFOs to execute a test method having of a series of steps. Upon execution, the steps cause the FIFO to manifest a variety of faults. This test method manifests faults by monitoring the outcome of operations and the values of particular flags indicative of normal FIFO operation. As correctly recognized by the Examiner, the method does not include sequentially extracting p test words from the memory plane and comparing them with the expected binary data bits.

The Martens et al. patent is directed to a dynamic scannable latch circuit for high-speed memory arrays utilized in high performance integrated circuit devices, wherein the high-speed memory arrays include data-bearing bitlines. The dynamic scannable latch circuit includes a group of scannable latch circuits for serially reading data from high-speed memory arrays during memory-testing cycles wherein each scannable latch circuit provides a scan output to a scan input of a second or next scannable latch circuit in a series of scannable latch circuits.

First, Appellants maintain that the Examiner has mischaracterized the Martens et al. reference. Marten et al. teaches that the array has the capability of reading data out serially in certain testing conditions. As such the memory elements are connected in series. However, nothing in Marten et al. discloses testing a sequential access memory plane by extracting test words sequentially from the memory plane to compare with expected binary data bits, as claimed.

Furthermore, none of the other cited references (Zorian et al. or Biskup et al.), relied upon by the Examiner as teaching various features such as a checkerboard pattern

and specific circuit implementation, makes up for the deficiencies of the Kim et al. and Marten et al. references as discussed above.

Additionally, Appellants maintain that the Examiner is impermissibly using the teachings of Appellants' own patent application as a roadmap to modify the prior art. For example, as noted above, both Kim et al. and Marten et al. teach the use of a memory test that does not include extracting test words sequentially from the memory plane to compare with expected binary data bits. It is Appellants disclosure that teaches such a feature.

On page 7 of the final Office Action, the examiner asserts that it would have been obvious to modify the method and apparatus of Kim et al. to include the scan register configuration and capability of Martens so that data could be read out of the Kim et al. apparatus serially or sequentially. However, the Examiner does not point to any suggestion that the skilled artisan would have been motivated to modify the Kim et al. apparatus. Indeed, the method and apparatus of the Kim et al. reference already provides reliable testing of all types of memories (Col. 2, lines 32-49 of Kim et al.).

As the Examiner and Board are aware, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim features. The initial burden is on the Examiner to provide some suggestion of the desirability of doing what the Applicants have done. To support the conclusion that the claimed invention is directed to obvious subject matter, either the reference must expressly or impliedly

suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Both the suggestion to make the claimed combination and the reasonable expectation of success must be founded in the prior art and not in Applicants' disclosure.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Furthermore, no proper combination of the teachings of the references could result in the invention as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 9, 11, 14, 20 and 26. Thus, the rejections under 35 U.S.C. §103(a) should be reversed.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above.

Claims 18, 24 and 30 are Patentable Over Kim et al. in view of Martens and Zorian et al.

Dependent Claims 18, 24 and 30 each recite that the first test circuit or means writes the test words to obtain a checkerboard test binary configuration in the memory array, and the test logic further includes an expected bit generator or means for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

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The Examiner points (page 9 of the final Office Action) to the Test pattern Generator (TPG) 118 of Kim et al. as allegedly meeting the claimed feature of the expected bit generator or means for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read, as claimed. The Examiner specifically references column 6, lines 23-36 of Kim et al., and reprodcued below, as teaching this claimed feature.

> The BIST capability is provided by a BIST control 122. The BIST control 122 controls a Test Pattern Generator (TPG) 118 and a Output Data Evaluator (ODE) 120. The TPG 118 generates test patterns, in the form of vectors, for input to the RAM 102. The test patterns from the TPG 118 are multiplexed by a multiplexer 121 with signals appearing on the Data Input (DI) line. The multiplexer 121 acts as a selector between the TPG 118 and the DI line. The function of the multiplexer 121 depends on whether the FIFO 100 is being tested. More particularly, during testing intervals, the multiplexer 121 passes test patterns from the TPG 118 to the DIR 108 for input to the RAM 102. During non-testing intervals, the multiplexer 121 passes signals received on the DI line to the RAM 102.

As can be seen from a reading of the cited portion of Kim et al., there is no teaching that the TPG 118 sequentially generates the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read, as claimed.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Furthermore, no proper combination of the teachings of the references could result in the invention as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 18, 24 and 30.

Thus, the rejection under 35 U.S.C. §103(a) should be reversed.

Claims 19, 25 and 31 are Patentable Over Kim et al. in view of Martens, Zorian et al. and Biskup et al.

Dependent Claims 19, 25 and 31 each recite that the test logic further includes an expected bit generator or means for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read. Furthermore, the generator/means includes a first bit generator/delivery means for generating a least significant bit of each read address, a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array, a second bit generator/delivery means for generating a least significant bit of each binary word in the counter, and a logic gate (EXCLUSIVE OR or EXCLUSIVE NOR) comprising two inputs connected to respective outputs of the first and second bit generators, and an output sequentially delivering the expected data bits.

Firstly, Appellants reiterate the arguments set forth above with respect to Claims 18, 24 and 29. Secondly, Appellants point out that the Examiner acknowledged that the Kim et al. reference does not teach that the TPG 118 includes a first bit generator/delivery means for generating a least significant bit of each read address, a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array, a second bit generator/delivery means for generating a least significant bit of each binary word in the counter, and a logic gate (EXCLUSIVE OR or EXCLUSIVE NOR) comprising two inputs connected to respective outputs of the first and second

bit generators, and an output sequentially delivering the expected data bits, as claimed.

However, the Examiner relies upon the Biskup et al. reference as allegedly teaching the details of the claimed expected bit generator. The Biskup et al. reference is directed to methods and an apparatus that provide a built-in error check in a disk drive. The methods and apparatus of Biskup et al. can detect a logical block address assigned to a portion of the platter of the hard drive and thereby detect when an erroneous seek has occurred. As is clear from the reference, the teachings have nothing to do with testing a sequential access memory array.

Moreover, the Biskup et al. reference teaches the use of a Logic Block Address (LBA), XOR gates and a least significant bits (LSB) in an approach to reveal any defects in the error checking circuitry (Col. 11 of Biskup et al.). Nothing in the Biskup et al. reference suggests the use of test logic including an expected bit generator for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read at all, much less the generator/means including a first bit generator/delivery means for generating a least significant bit of each read address, a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array, a second bit generator/delivery means for generating a least significant bit of each binary word in the counter, and a logic gate (EXCLUSIVE OR or EXCLUSIVE NOR) comprising two inputs connected to respective outputs of the first and second bit generators, and an output sequentially delivering the expected data bits.

There is simply no teaching or suggestion in the

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cited references to provide the combination of features as claimed. Furthermore, no proper combination of the teachings of the references could result in the invention as claimed. Accordingly, for at least the reasons given above, Appellants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 19, 25 and 31. Thus, the rejection under 35 U.S.C. §103(a) should be reversed.

CONCLUSIONS

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable decision by the Examiner.

Respectfully submitted,

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I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to: MS Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 19 day of September, 2005.

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APPENDIX A - CLAIMS ON APPEAL
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9. (Previously presented) A method of testing a sequential access memory array for storing p words each of n bits, the method comprising:

writing p test words each made up of n test bits in the memory array;

sequentially extracting the p test words from the memory array; and

comparing the test bits of the extracted test words with expected data bits so that for each test word extracted, the corresponding n test bits are compared sequentially with n respective expected data bits before extracting the next test word.

10. (Previously presented) A method according to Claim 9, wherein the p test words each of n bits are written in such a way as to obtain a checkerboard test binary configuration in the memory array; and further comprising sequentially obtaining the expected data bits by respectively logically combining read addresses of the test words and ranks of the test bits of each test word that is read.

11. (Previously presented) A method of testing a sequential access memory array, the method comprising:

writing test words each made up of a plurality of test bits in the memory array;

sequentially extracting the test words from the memory array; and

comparing the test bits of the extracted test words with expected data bits so that for each test word extracted, the corresponding test bits are compared sequentially with

respective expected data bits before extracting the next test word.

12. (Previously presented) A method according to Claim 11, wherein writing test words in the memory array comprises forming a checkerboard test binary configuration in the memory array.

13. (Previously presented) A method according to Claim 12, further comprising sequentially obtaining the expected data bits by respectively logically combining read addresses of the test words and ranks of the test bits of each test word that is read.

14. (Previously presented) A sequential access semiconductor memory device comprising:

a memory array for storing p words each of n bits; and

test logic connected to n outputs of the memory array and including

first test means for writing p test words each having n test bits in the array, and

second test means for sequentially extracting the p test words from the memory array and, for each extracted test word, sequentially comparing the corresponding n test bits with n expected data bits, before extracting the next test word.

15. (Previously presented) The device according to Claim 14, wherein the second test means comprises:

a set of n connected output registers connected to n respective outputs of the memory array;

first control means for delivering a first control

signal to the output registers to simultaneously store the n test bits of a current test word in the output registers;

second control means for delivering a second control signal to the output registers to sequentially shift the test bit contained in each connected output register toward the next connected output register and to sequentially extract the n test bits of the current test word from a last connected output register of the set; and

comparator means for comparing each bit extracted from the last connected output register with the corresponding expected data bit.

16. (Previously presented) The device according to Claim 15, wherein each output register comprises a D-type flip-flop having a data input connected to one of the n outputs of the memory array, a test input, a test output and a test control input for receiving successively and alternately the first control signal and the second control signal; the test output of each flip-flop being connected to the test input of an adjacent flip-flop, the test input of a first flip-flop of the set being receiving an initial data bit, and the test output of the last flip-flop of the set being connected to a first input of the comparator means.

17. (Previously presented) The device according to Claim 16, wherein the comparator means comprises one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate.

18. (Previously presented) The device according to Claim 14, wherein the first test means writes the p test words each of n bits to obtain a checkerboard test binary configuration in the memory array; and the test logic further includes generator means for sequentially generating the

expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

19. (Previously presented) The device according to Claim 18, wherein the generator means comprises:

first delivery means for generating a least significant bit of each read address;

a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array;

second delivery means for generating a least significant bit of each binary word in the counter; and

one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate comprising two inputs connected to respective outputs of the first and second delivery means, and an output sequentially delivering the expected data bits.

20. (Previously presented) A sequential access semiconductor memory device comprising:

a memory array; and

test logic connected to the memory array and including

a first test circuit for writing test words each having a plurality of test bits in the array, and

a second test circuit for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

21. (Previously presented) The device according to

Claim 20, wherein the second test circuit comprises:

a set of connected output registers connected to respective outputs of the memory array;

a first control device for delivering a first control signal to the output registers to simultaneously store the test bits of a current test word in the output registers;

a second control device for delivering a second control signal to the output registers to sequentially shift the test bit contained in each connected output register toward the next connected output register and to sequentially extract the test bits of the current test word from a last connected output register of the set; and

a comparator for comparing each bit extracted from the last connected output register with the corresponding expected data bit.

22. (Previously presented) The device according to Claim 21, wherein each output register comprises a D-type flip-flop having a data input connected to one of the outputs of the memory array, a test input, a test output and a test control input for receiving successively and alternately the first control signal and the second control signal; the test output of the flip-flops being connected to the test input of an adjacent flip-flop, the test input of a first flip-flop of the set receiving an initial data bit, and the test output of the last flip-flop of the set being connected to a first input of the comparator.

23. (Previously presented) The device according to Claim 22, wherein the comparator comprises one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate.

24. (Previously presented) The device according to

Claim 20, wherein the first test circuit writes the p test words each of n bits to obtain a checkerboard test binary configuration in the memory array; and the test logic further includes an expected bit generator for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

25. (Previously presented) The device according to Claim 24, wherein the generator comprises:

a first bit generator for generating a least significant bit of each read address;

a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array;

a second bit generator for generating a least significant bit of each binary word in the counter; and

a logic gate comprising two inputs connected to respective outputs of the first and second delivery circuits, and an output sequentially delivering the expected data bits.

26. (Previously presented) A test circuit for a sequential access semiconductor memory device having a memory array, the test circuit comprising:

a first test circuit for writing test words each having a plurality of test bits in the array; and

a second test circuit for sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

27. (Previously presented) The circuit according to Claim 26, wherein the second test circuit comprises:

a set of connected output registers connected to respective outputs of the memory array;

a first control device for delivering a first control signal to the output registers to simultaneously store the test bits of a current test word in the output registers;

a second control device for delivering a second control signal to the output registers to sequentially shift the test bit contained in each connected output register toward the next connected output register and to sequentially extract the test bits of the current test word from a last connected output register of the set; and

a comparator for comparing each bit extracted from the last connected output register with the corresponding expected data bit.

28. (Previously presented) The circuit according to Claim 27, wherein each output register comprises a D-type flip-flop having a data input connected to one of the outputs of the memory array, a test input, a test output and a test control input for receiving successively and alternately the first control signal and the second control signal; the test output of the flip-flops being connected to the test input of an adjacent flip-flop, the test input of a first flip-flop of the set receiving an initial data bit, and the test output of the last flip-flop of the set being connected to a first input of the comparator.

29. (Previously presented) The circuit according to Claim 28, wherein the comparator comprises one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate.

30. (Previously presented) The circuit according to Claim 26, wherein the first test circuit writes the p test

words each of n bits to obtain a checkerboard test binary configuration in the memory array; and the test logic further includes an expected bit generator for sequentially generating the expected data bits from respective logical combinations of read addresses of the test words and ranks of the test bits of each test word that is read.

31. (Previously presented) The circuit according to Claim 30, wherein the generator comprises:

a first bit generator for generating a least significant bit of each read address;

a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array;

a second bit generator for generating a least significant bit of each binary word in the counter; and

a logic gate comprising two inputs connected to respective outputs of the first and second delivery circuits, and an output sequentially delivering the expected data bits.